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The Impact of Switching Capacitor Banks with Very High Inrush Current on Switchgear

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SUMMARY

Capacitor banks are installed in an increasing number in order to control power quality issues in the transmission and distribution networks. Due to load fluctuation, switching of capacitor banks is normally a daily operation. Although the current to be switched (e.g. the normal load current) is far below the maximum capability of circuit breakers, the transient current upon making (the so-called inrush current) has proven to be a major challenge for circuit breakers.
The often very high value of (inrush) current flowing during the closing (pre-) arc between breaker contacts is potentially harmful for the contact system. The IEC circuit breaker 62271-100 standard specifies 20 kA peak while energizing (an) additional bank(s) to those already energized, the so-called back-to-back configuration.
It will be demonstrated that three-phase energization with full inrush current cannot be reliably performed in test-circuits.

Statistics will be presented on the number of (transmission, distribution) circuit breakers that were tested for this duty. The probability of a late breakdown in vacuum, after energization with inrush current, is rising with rated voltage. Absence of late breakdown of vacuum interrupters after capacitive current switching is especially challenging at higher voltage levels, and is a main barrier to develop vacuum interrupters for transmission voltages having very low probability of re-strike.
It was observed that in SF6 circuit breakers, the very intense pre-arc can damage the nozzle, whereas in vacuum circuit breakers, the inrush current arc may deteriorate the dielectric withstand of the switching gap, sometime leading to (late) breakdown after load current interruption.

A new measurement method is described to monitor the field electron emission (FEE) current that flows in a pulsating manner in vacuum gaps after current interruption. This measurement system is able to deal (and measure) currents varying as wide as nine decades, from full breakdown currents of several tens of kA to FEE currents of tens of μA). Research tests in full-power test-circuits (following the IEC standard) with a number of prototype vacuum interrupters of different geometry and contact material show a very large range (from micro-amperes to milli-amperes) of current during recovery voltage after load current interruption.

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It was observed that the load current at longer arcing times reduces the electrical emission activity of the contact surfaces. Large inrush current increases the FEE current.
No relationship between steady state FEE current intensity and breakdown probability could be established.

KEYWORDS

Breakdown, capacitive current, current measurement, electric field emission, inrush current, SF6 circuit breaker, standardization, switching, vacuum circuit breaker, testing, back-to-back.

1. SWITCHING OF CAPACITIVE LOADS

Unlike fault current switching, the interruption of capacitive current is a very standard switching situation [1]. The usual cases in which capacitive current is switched are the following:

1. Switching of unloaded overhead transmission lines or local station components. In this case, load is already rejected (e.g. by a breaker at the remote end of the line) but due to the stray capacitance of the overhead line system, a small current is still flowing in the system, to be interrupted by the station breaker.
2. Switching of cables. Due to the relatively high capacitance of cables (compared to overhead lines), the current to be interrupted is higher.
3. Switching of capacitor banks. Capacitor banks, because of their concentrated capacitance, generally draw much more current than unloaded cables or lines, in practical cases several hundreds of A. Regarding the interruption of current, switching of capacitor banks is principally no other switching duty than line- or cable switching. The main difference is the frequency of switching: whereas the switching of unloaded lines and cables is a rare event, the switching of capacitor banks is a very frequent operation, since capacitor banks are installed to supply reactive power on a night/day varying basis. Thus, the switching performance of capacitor banks has to be considered on a statistical basis, taking into consideration a very large number of switching operations.
   Regarding the energization of capacitor banks (the making), the concentrated nature of the capacitance causes another very tricky phenomenon for circuit breakers: this is the inrush current, a very high transient current, drawn by the capacitor bank. Since the surge impedance of capacitor banks is far smaller than that of cables and lines, capacitor bank inrush current (and its consequences) management is of considerable concern to users and developers of switchgear.

The typical features of capacitive load switching are:
- Current leads the voltage by 90 degrees, this means that at the moment of current zero the supply voltage is close to maximum;
- the load capacitance is charged to the voltage it had at current interruption and keeps this as a DC voltage. This implies that recovery voltage is basically a "1-cosine" wave shape having power frequency [2];
- current is much smaller than the rated (short-circuit) breaking current of the breaker. This implies that it is very easy for the breaker to interrupt the current (at least initially) even very shortly after contact separation, in those cases that contact separation is very close to current zero;
- for capacitor bank switching, the number of switching operations is very high, estimated as 120 switching operations per year [3];
- for capacitor bank switching, there exists a considerable inrush current upon energization.

The combination of short contact gap at current zero and high recovery voltage makes it possible for the breaker to re-strike (a breakdown of the open(ing) gap later than a quarter power frequency cycle after current interruption). At re-strike, the sudden release of the energy stored in the load, can lead to damage of the breaker 's contact system. Also, re-strike can lead to voltage escalation [2] that maybe harmful for other station equipment.

Breakdown earlier than a quarter power frequency cycle after interruption is called re-ignition, considered as a harmless phenomenon inherent to the interruption process.

On a statistical basis, capacitor bank switching is the most severe capacitive switching operation. Because of inrush the circuit breaker maybe conditioned negatively and because of the many switching operations the probability of re-strike during the breaker's lifetime is very high.

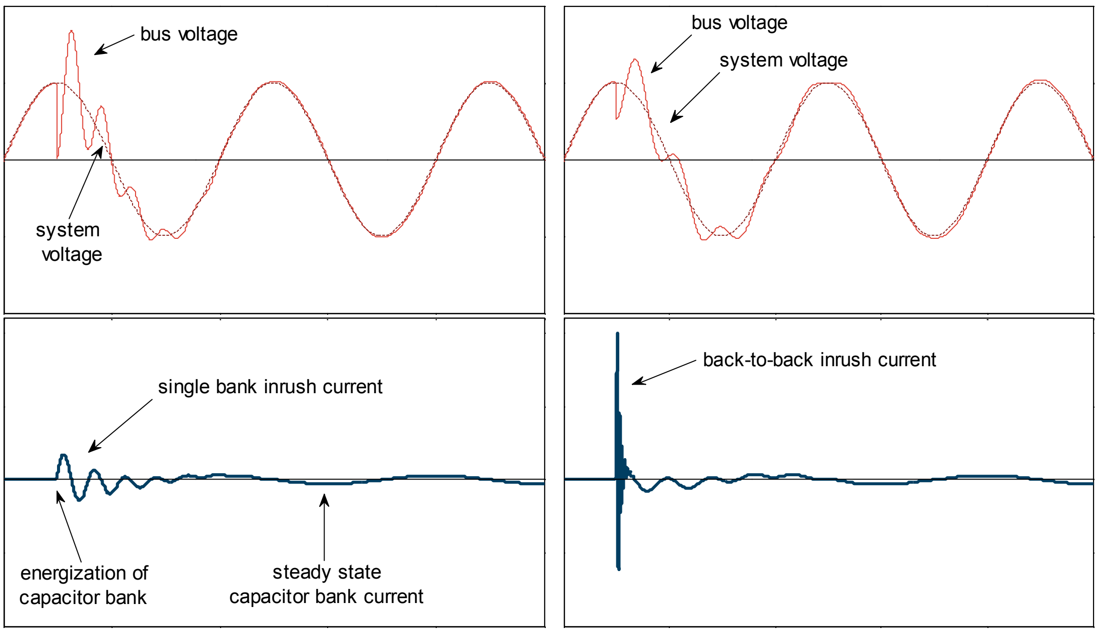

Fig. 1 Single cap bank energization (left) and back-to-back cap bank energization (right).
Top: Energization voltage transient on bus; bottom: Energization current transient through circuit (breaker)

2. CAPACITOR BANK ENERGIZATION

When a capacitive load is energized, it will usually draw a certain inrush current. In the case a lumped (uncharged) capacitor is connected to a voltage source, the sudden change (from zero to a certain value) in capacitor voltage du/dt has a very large value, leading to a very large current. The inrush current is proportional to the surge impedance of the (capacitive) load, and this is the reason that distributed "capacitances" such as cables and lines, with their relatively high surge impedances of several tens and several hundreds of ohms respectively, draw modest inrush current. Normally, the energization of cables and lines is not associated with inrush current and related challenges to the breaker [4].
This is not the case for capacitor banks. Surge impedances of capacitor (bank)s are just a few ohms, and very large inrush currents have to be expected at making.

The challenge of capacitor bank inrush current is two-fold:

- For the switching device: the inrush current starts to flow at the moment of pre-strike, before contact touch. Due to the high-frequency of the inrush current, the peak values of the current (and normally several periods) are easily reached during the pre-arc duration. This causes a stress to the interrupter. In gas, shock waves can result, and damage of internal parts (e.g. holes in nozzles in SF6 breakers) is observed from time to time. For vacuum breakers, during inrush current, the contacts are closing under intense arcing, causing the contacts to weld. Subsequent contact separation breaks the welds and draws micro-protrusions. When there is no or little arc activity after contact separation to "burn" these whiskers away, voltage withstand can be a challenge.
- For the system: depending on the capacitor bank's topology, voltage transients can arise at the station bus, potentially causing power quality issues [5].

The severity of both transients greatly depends on the circuit topology of the capacitor banks.

Two situations are normally distinguished:

- Single bank topology: herein, a single bank is energized without other banks already connected to the bus. In a simplified approach, it can be assumed that the inrush current is flowing mainly through the circuit's short-circuit reactance. The advantage is that this reactance limits the inrush current, but the drawback is that the bus voltage is strongly affected by the switching operation, resulting in a severe bus voltage excursion. Electrically, the situation is shown in figure 1 (left). Severe bus transients can occur, and peak inrush current is several kA, with a modest frequency of several hundreds of Hz. In the single bank situation, due to the bus voltage transients switching imposes power quality stresses mainly to the system, not to the breaker.
- Back-to-back topology: herein, a single bank is energized with other banks already connected to the bus. Now, the inrush current mostly flows through (the) neighbouring bank(s). In this situation, the inrush current is only limited by the (stray) inductance of the banks' connection, but no longer mainly flows through the source circuit. The advantage is an almost undisturbed bus voltage, whereas the breaker endures a very large inrush current. The electrical impact is shown in figure 1 (right side), where the inrush current is 20 kA peak, with a frequency of several kHz.
  In practice, inrush current can be several to many tens of kA peak at several kHz.
  In the back-to-back situation, capacitor bank energization imposes stresses mainly to the breaker, less to the system.

In order to mitigate the effects of inrush current, the following measures are often considered:

1. Adding a reactor in series with the capacitor bank. Its reactance reduces the inrush current, as well as the re-strike current – in case of re-strike.
2. Application of synchronized (controlled) switching. In this case, the energization is chosen to coincide with the relevant voltage zero crossings in each of the phases, leaving virtually no inrush current. Although this method is widely applied, it will not reduce the re-strike current (normally larger than the inrush current).
3. Non-linear elements, by which a damping resistor is only inserted during the inrush period [6].

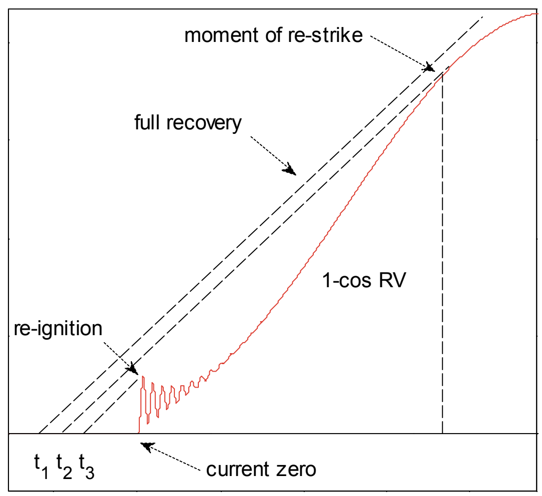

Fig. 2: Re-ignition and re-strike in relation to voltage jump

Stress imposed by capacitor bank switching was studied by CIGRE WG 13.04 [7] and is presently under renewed investigation by CIGRE WG A3.26 ("Capacitor bank switching and impact on equipment").

3. STANDARDIZATION STATUS

The standardized requirements of capacitor bank switching are laid down in IEC 62271-100 [8] and IEEE C37.09a [9]. Relevant application guides are CIGRE TB 305 [10] and IEEE Std. C37.12-2005 [11].
The relevant test-requirements are summarized in table 1.

The standards make a distinction between two classes of capacitive switching performance:

- C1: Low probability of re-strike, to be verified by the number of test as specified in the columns 3-phase and 1-phase. A single re-strike is allowed in the test-series BC1+BC2; if there are two re-strikes a repetition of the complete series is permitted, but with no more than one additional re-strike.

- C2: Very low probability of re-strike. This needs a higher number of tests in comparison to the C1 class. A single re-strike is permitted in test-series BC1+BC2, but this needs a repetition of the test-series without re-strike. In addition, to simulate ageing the breaker must be pre-conditioned with three opening operations at 60% of the rated short-circuit current (or the T60 duty [8]).

Class C1: low probability of re-strike								
test duty	pressure	current	operation	jump	3-phase		1-phase	
BC1	rated	40 – 160 A	O	<2 %	24 O	6 O*	24 O	6 O*
BC2	rated	≥ 400 A	CO	<5 %	24 CO	6 O*	24 CO	6 CO*
no pre-conditioning								
three re-strikes allowed incl. repetition of total series								

Class C2: very low probability of re-strike								
test duty	pressure	current	operation	jump	3-phase		1-phase	
BC1	minimum	40 – 160 A	O	2%	24 O	12 O*	48 O	12 O*
BC2	rated	≥ 400 A	CO	5%	80 CO	64CO*	120 CO	84CO*
additional pre-conditioning with 3 times T60 current								
one re-strike allowed; repetition of total series must be re-strike-free								

*Table 1: Standardized requirements for circuit breakers to pass IEC / IEEE capacitor bank switching test-duties. *: Number of tests to be carried out at minimum arcing time*

An important aspect of testing is the correct representation of the voltage jump (column "jump" in table 1). Voltage jump is the initial (transient) part of the recovery voltage, originating from the supply system. The amplitude of the voltage jump (ΔU, given by IEC as the voltage variation in % at switching) is simply given as:

$\Delta U \approx Ib/Isc = Q/P$, with Ib, Isc the rated cap bank current and the rated short-circuit current, P the local short-circuit power and Q the cap-bank power. In figure 2, this voltage jump (together with the 1-cos recovery voltage) is drawn together with three (schematically) recovery curves, suggesting the increase in breakdown voltage of the opening switching gap.

This is to illustrate the relationship between arcing time, re-ignition / re-strike probability and voltage jump amplitude: very short arcing time (contact separation after t_3) leads to re-ignition in the sketched case, a slightly longer arcing time (separation at t_2) shows re-strike and any contact separation before t_2 (e.g.t_1) leads to full recovery. From this, it is clear that a higher value of ΔU has a lower probability of re-strike. This, in turn, implies that capacitive switching tests must be performed with a sufficient strong short-circuit source at supply side, even though the actual capacitive current is very small.

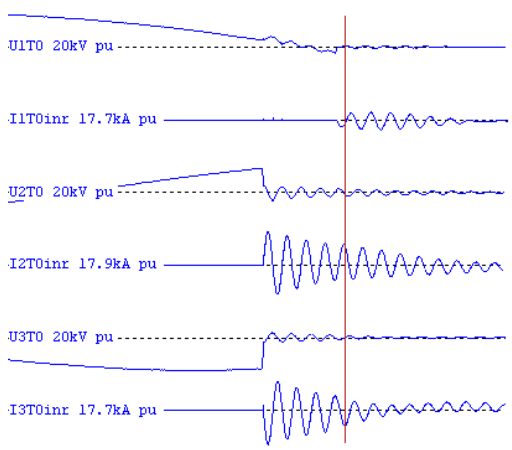

Fig. 3: Three-phase inrush current in lower two phases only

In the back-to-back configuration the C (closing) operation has to be performed with a circuit providing an inrush current of 20 kApeak at a frequency of 4250 Hz for all rated voltages.

4. TESTING

The realization of the standardized value of inrush current (20 kApeak at 4250 Hz) in testing is a challenge. In order to produce the very high inrush current at the required frequency, the test-circuit part providing the inrush current must have an extremely low surge impedance. This implies that, especially for the lower rated voltages, where capacitor bank have a limited charging voltage, very compact test-circuits must be constructed in order to minimize the circuit's stray inductance. Realization of the extreme values of inrush current up of several tens of kA, as stipulated in the IEEE standard [12], is impossible at the lower rated voltages. In very limited situations, synthetic test circuits could be used.

For the performance of three-phase tests, three inrush current providing cap banks are required. The main problem, however, of generating three-phase inrush current is the very little control of the pre-strike moment. In ungrounded cap bank systems, full inrush currents will only develop after pre-strike of at least two phases, with maximum phase-to-phase voltage across the gaps. In the third phase to pre-strike, the inrush current is always well below the value required in the standards. In figure 3, a measurement is given, showing the sequence of inrush current in a three-phase test-situation.
Because the pre-strike of circuit breaker gaps will often occur at an unexpected moment and depends very much on the mechanical behaviour of the breaker, three-phase inrush current testing is considered impractical.

As a compromise between three-phase and single phase testing, KEMA has developed a test-circuit that generates a full and well-controlled inrush current in one phase (the first-phase-to-clear), whereas the opening operation is under full three-phase conditions.
The advantage with respect to single phase circuits is a realistic recovery voltage, since in single phase tests the source voltage must be increased (expressed by the multiplication factor e.g. $k_c = 1.4$ [8]) in order to have correct coverage of the first-pole-to-clear condition. The drawback of single phase tests is then the presence of the first-pole-to-clear increased voltage not only during the first pole to clear but during the full recovery phase.

5 CAPACITOR BANK TEST STATISTICS

KEMA has evaluated all its capacitor bank tests in the period June 2000 – February 2011, 433 test series (completed test-duties BC1, BC2) in total, in a rated voltage range 12 – 550 kV from 72 different manufacturers / manufacturing sites. After detailed evaluation, 297 test-series were documented sufficiently to take part in the present survey.
The test-series are classified and counted as follows:

Category	Description	number
I	Test series are part of certificate	130
II	Test-series are part of certificate – single re-strike occurred	10
III	Not part of a certificate issued*	132
IV	Not part of a certificate issued*, multiple re-strikes occurred	25
V	Insufficient information available to be classified in the categories above	136
	Total test series studied	433
* Certificate proving capacitive switching capability implies certificate on making and breaking performance is also present. Absence of switching performance certificate (category III) might be due to unsatisfactory performance at short-circuit duties, not necessarily due to unacceptable capacitive switching performance		

Table 2: Population of test-result statistics

Of the 124 series, being part of a certificate and mentioning a class of capacitive switching performance, 102 had C2 class (from which 19 had the back-to-back configuration tested) and 22 a C1 class (2 back-to-back tested).

A breakdown of the various categories I-IV to rated voltage, distinguishing between single bank and back-to-back is shown in figure 4. One (or more) re-strike(s) were observed in 35 test-series making 11.3% of all test-series having conclusive information. A breakdown to voltage (medium and high) and cap bank configuration (single bank or back-to-back) does not show a difference in re-strike occurrence.
This is visualized in figure 5 (top). Due to the relatively small number, no evident conclusion can be given on the difference in occurrence in single bank and back-to-back test-series

One (or more) NSDDs (non-sustained disruptive discharges) were observed in 74 test-series (in 51 single bank test series and in 23 back-to-back series). All NSDDs occurred in test-objects having a rated voltage up to and including 40.5 kV.
Defining three ranges of voltages in the medium voltage range, the observed occurrence of NSDDs as a fraction of all relevant test-series in that voltage class is given in figure 5 (bottom). This figure suggests a very high occurrence of NSDD in back-to-back tests in the higher medium voltage class.

Since the vast majority of the tested switchgear up to and including 40.5 kV is vacuum switchgear, these results confirm that NSDD is a phenomenon inherent to vacuum interruption only. No NSDD was observed in SF6 switchgear. NSDD occurs in 37% of the documented test-series, so it is not a rare phenomenon. This confirms earlier studies [13] that reports NSDD occurrence in 32% of all KEMA vacuum switchgear test reports (including short-circuit tests) issued in 1999.

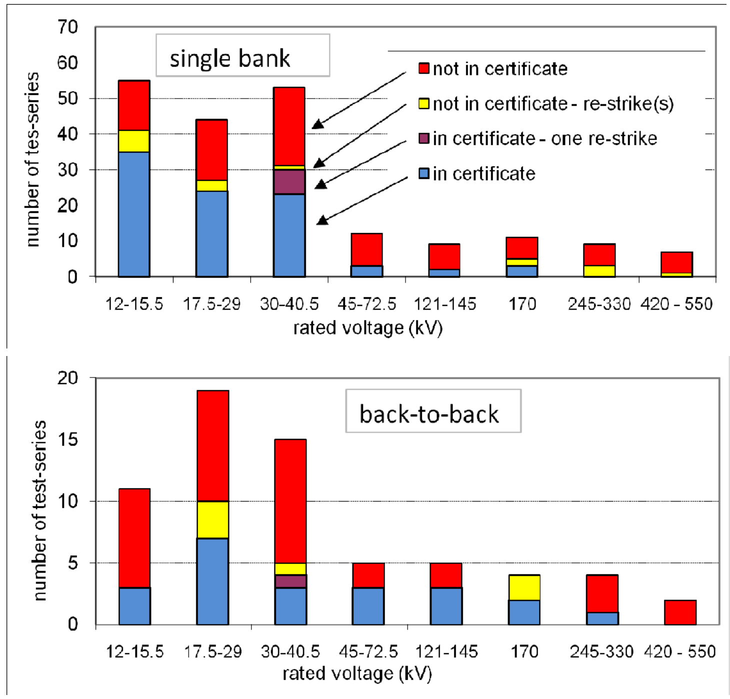

Figure 4: Numbers of cap bank test-series in voltage classes for single bank (top) and back-to-back (bottom) tests.

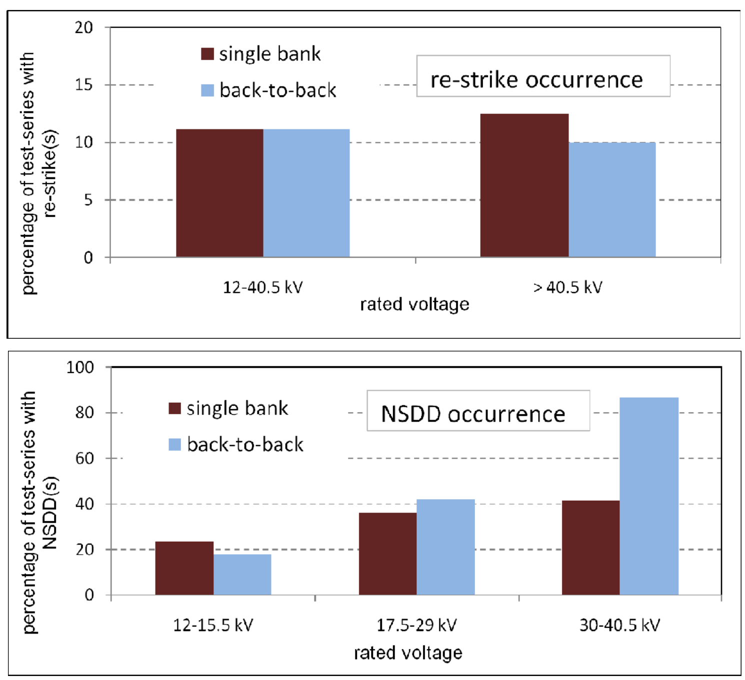

Fig. 5: Percentage of test-series in which re-strike (top) and NSDD (bottom) occurred..

6. STRESSES TO BREAKERS

Inrush current starts to flow at the moment the breaker's contact gap pre-strikes. From that moment on, the pre-arc will start and inrush current supplies the pre-arc until galvanic touch. Depending on the frequency of the inrush current and the duration of the pre-arc period, very high current values can flow during the pre-arc.
Figure 6 shows the arc energy (assumed to be proportional to the integrated current) for closing into an IEC back-to-back inrush current of 20 kApeak, a symmetrical and asymmetrical fault current of 50 kA. From this, it is clear that the arc energy and especially the rate of energy supply is very large under back-to-back inrush conditions.

SF6 circuit breakers will face major stresses to their contact system upon pre-strike when followed by inrush current having a rate of rise of hundreds of A/us in the back-to-back situation (as compared to the several tens of A/us) during closing into a fault current. The steep rising current will lead to extremely rapid heating and gas expansion in the inter-contact gap causing shock waves. The dielectric coordination between main contacts and arcing contacts during making must be such that pre-strike occurs under all circumstances only between the arcing contacts. Due to the high-capacitor discharge frequency, the skin-effect forces the arc foot points to burn near the stationary arcing contact circumference instead of causing a homogeneous erosion of the contact material. As a result, after many switching operations, the contact gets a conical structure, instead of a more hemi-spherically rounded one as with fault current making [14]. The conical structure, in turn, has been observed to increase the probability of pre/re-strike between the main contacts. This can lead to malfunction of the breaker [15].

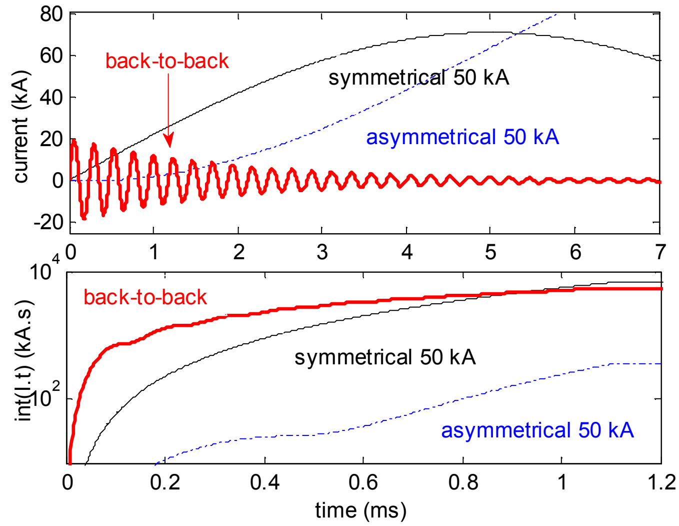

Fig. 6: Currents (top) and integrated current (bottom) during pre-arcing period

In several cases, during the required visual contact inspection after back-to-back testing punctures where found in the nozzle of high-voltage breakers, even without re-strikes [16]. Such punctures are detrimental for the pressure build-up, necessary for fault current interruption.

Vacuum circuit breakers do not have separate main- and arcing contacts. This implies that (pre-strike) arcing is on the same contacts that have to withstand the voltage in open position. Due to the back-to-back pre-strike arc, the very high current causes local contact melting, and during touch contacts often weld locally. The contact mechanism should be designed to break this weld, but remnants of the weld may cause local surface irregularities that act as electrical field enhancing sites. If these (micro-)

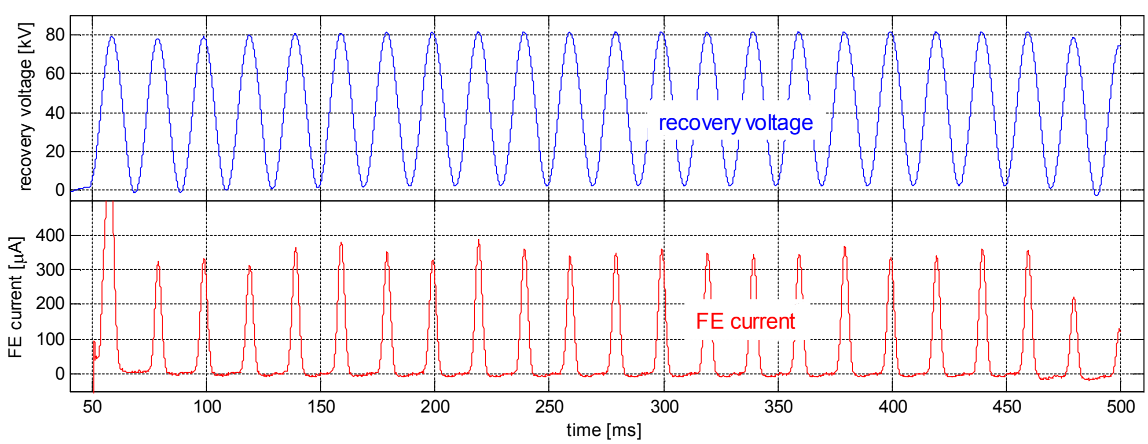

Fig. 7: Field electron emission current (bottom) during recovery voltage (top) of 36 kV vacuum interrupter after interrupting 400 A capacitive current with making at 20 kA back-to-back inrush current

protrusions are not sufficiently removed by arcing during the opening of the contacts, they may impair the dielectric strength of the contact gap. Thus, higher currents during switching off and/or longer arc duration reduce the effect of weld remnants.

A common failure mode in testing is welding after closing (contacts stick together). Also, the observed high probability of NSDD during back-to-back testing (see fig. 5) may be explained by an impaired dielectrical integrity due to pre-arcing and subsequent welding.
The scientific community presently considers two mechanisms at the origin of vacuum breakdown: electron field emission- and particle induced breakdown. Research into the breakdown mechanism shows that micro-particles detached from protrusions formed by separating the welded contacts are the main cause of re-strike [17, 18]. The conclusion of the present publication is that electron emission only cannot be the sole cause of vacuum breakdown.

7. VACUUM FIELD ELECTRON EMISSION CURRENT MEASUREMENT

Capacitive current switching is a very common, but at the same time one of the toughest switching duties for a vacuum circuit breaker, because the switching modifies the contact surface in an unfavourable way [19].
In order to get more insight into the effect that back-to-back currents have on the surface topology (and the related dielectrical impact) of vacuum interrupters, a method was developed to measure the electron field emission current during recovery after capacitive current interruption, including making with full IEC standardized back-to-back inrush current [20]. Field electron emission (FEE) current arises as a result of extremely high electrical fields allowing electrons to "tunnel" through the metallic surface potential barrier. The extremely high electrical fields results from local surface topology including very sharp edges, ridges, protrusions, pores, cracks etc. Field enhancement factors in the range 600-1000 were observed in practical vacuum interrupters even without closing on high-inrush current [20].

7.1 Measurement

The method, originally designed for application in a research laboratory was adapted to be applicable in KEMA's high-power laboratory. Therefore, the original analogue, on-line data processing was replaced by off-line digital data processing and the data acquisition system was made suitable for application under strong EM polluted environment at any potential of the current measurement sensor. The lower limit of measurable FEE current is 30 uA. This implies the measurement system is able to deal with a dynamic range of more than 9 decades: from 30 uA up to 50 kA in case of re-strike. Figure 7 shows an impression of a typical measurement. Note the very rapid decrease of FEE current at slightly lowing of the recovery voltage near the end of the wave traces, indicating the exponential dependence of FEE current with applied voltage [21].

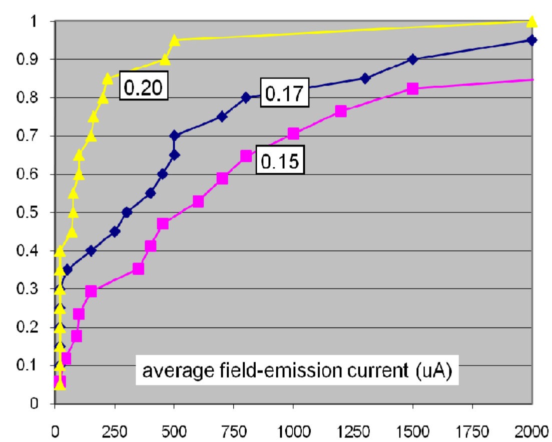

Fig 8: Cumulative "smaller than" plot of FEE current in three interrupters. Indicated figures are fraction of test with re-strikes

7.2 Tests

Nine prototype vacuum interrupters with different design and contact material (in three identical circuit breakers) were used in the investigation. All tests were performed in a single phase test-circuit designed for 400 A capacitive current in36 kV rated voltage and IEC back-to-back requirement (20 kApeak at 4250 Hz). All vacuum interrupters were preconditioned with 60% short-circuit current, as required for class C2.
The contacts of one interrupter welded already at the first tests. In the other 8 interrupters, 15 re-strikes were observed in 125 full CO tests. The range of observed FEE current is up to 4000 uA. Usually, the first peak of FEE current is significantly higher than the following ones (see for example fig. 7 and 10).

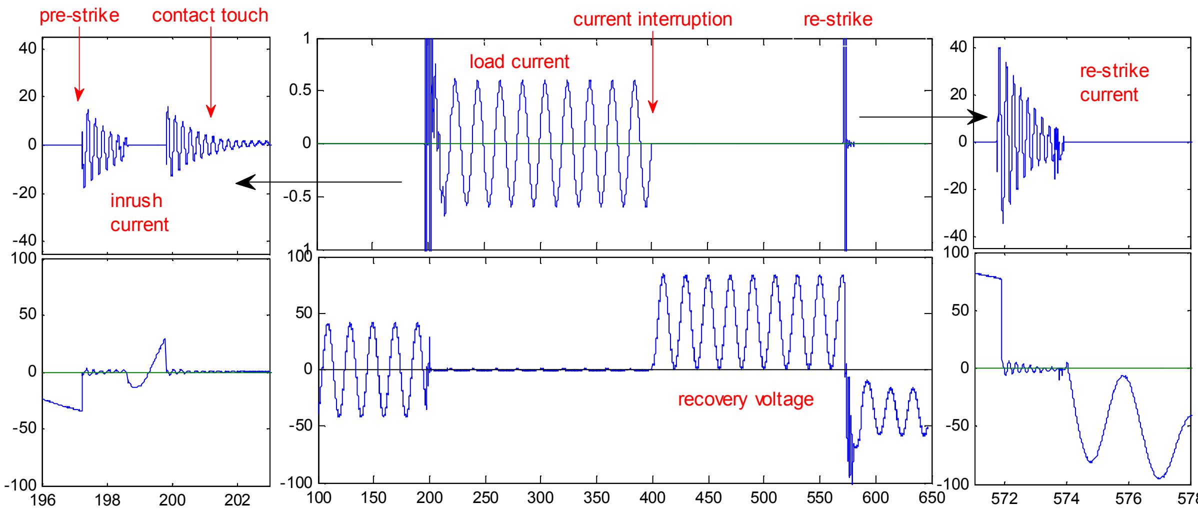

Fig 9: Current (top, [kA] and voltage across the interrupter (bottom, [kV]) during a single phase back-to-back test. Time in ms. Left: Pre-arcing period enlarged, middle: complete sequence , right: re-strike period enlarged.

In one case, measurable FEE current started only after 90 ms, without re-strike even appearing.

When considering the wide variety of measured FEE signals, there appears no one-to-one relationship between average FE current level during the recovery period and re-strike occurrence. There were cases with FEE current as high as 1100 uA without re-strike and cases with FEE current below the measurement threshold still showing re-strike.

Nevertheless, a statistical approach reveals differences in FEE emission activity between interrupters. An example of this is figure 8, showing the cumulative distribution of FEE current for three different interrupters (in the same breaker) presenting the same design but different contact material. The annotated figures give the fraction of tests with re-strike. As can be seen, there is no relationship between FEE current magnitude and re-strike probability.

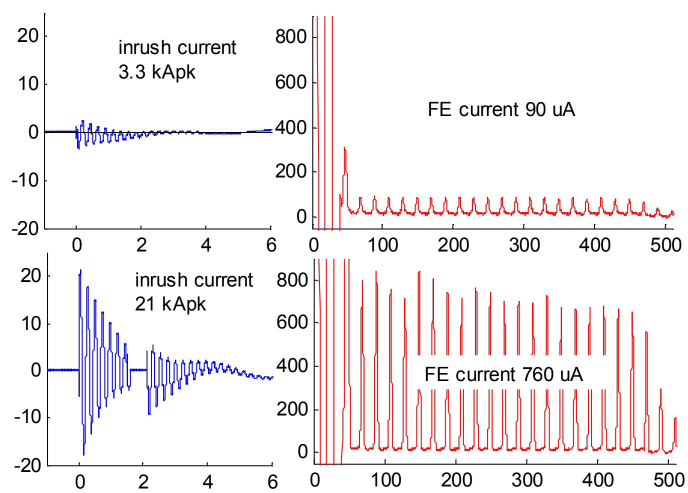

Fig 10: Effect of low (top) and high (bottom) inrush current on FEE current after interruption of 400 A capacitive current

7.3 Effect of inrush current.

In many cases, the vacuum interrupter can interrupt the inrush current because of the inherent property of "vacuum" to interrupt current of very high di/dt. This leads to a currentless period during pre-"arcing". During the absence of arcing in this period, however, the capacitor bank recharges again and the subsequent breakdown starts from a high value. This is visualized in fig. 9 (measured result). In such cases, the inrush current creates an additional stress (higher arc energy) to the interrupter. Note the re-strike in this test at 171 ms after current zero. There was no early warning sign from elevated FEE current prior to this event. Because the re-strike was near recovery voltage maximum, the re-strike current was with 39 kApeak nearly the double of the inrush current.

There exists a clear relationship between inrush current magnitude and FEE current level.

In all cases with lower inrush current (< 10 kApeak) there was a lower FE current. The opposite, however, is not true: high inrush current (20 kApeak) do not necessarily lead to high FEE current level. Figure 10 gives an impression of typical tests with low (top) and high (bottom) inrush current and the resulting FEE current.

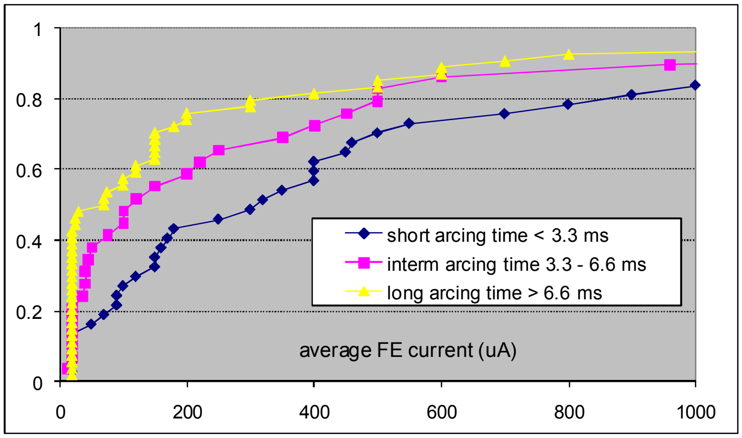

Fig. 11: Cumulative "smaller than" plot of FEE current for three classes of arcing time.

7.4 Conditioning effect.

After contact separation, the rated capacitive current arc is assumed to have a positive conditioning effect on the vacuum interrupter contact surfaces [22, 23]. Generally, the surface becomes "smoothed" because of the thermal action of the small arc cathode spots (foot points). The higher the rated capacitive current and the longer its duration (arcing time) the more effective the arc conditioning works. Higher (capacitive) current means more cathode spots and longer arcing time means a larger surface area is potentially covered by cathode spots. Thus, the adverse effect of broken inrush current welds on the dielectric properties will be counteracted to a certain degree. The effect of arc duration on FEE current could be demonstrated by measurement. In figure 11, the cumulative "smaller than" distribution of FEE current is plotted for short arcing time (< 3.3.ms), intermediate arcing time (3.3 – 6.6 ms) and long arcing time (> 6.6 ms). From this, statistically an effect of arc conditioning by longer arcing time is suggested. Note that at long arcing times, in nearly 50% of the cases the FEE current remains below the threshold of the measurement.

8. CONCLUSIONS

- High inrush currents during the energization of a capacitor bank while (an)other parallel bank(s) are already in service (back-to-back configuration) causes severe stresses to the contact system of circuit breakers.
- SF6 breakers must be designed to withstand severe mechanical shockwaves and may experience uneven wear of arcing contacts
- In KEMA test-experience, in around 10% of all capacitor bank tests, re-strikes are observed. Late, self-restoring breakdown events (NSDD) occur much more frequently, but exclusively in vacuum interrupters and very frequently during back-to-back switching at rated voltages > 30 kV.
- Vacuum breakers face unfavourable contact micro-topological changes due to local welding of contacts during making operations in the presence of inrush current..
- Electron field emission alone cannot be the root cause of re-strike in capacitive switching: There is no clear relation between (steady state) field emission current intensity and probability of re-strike.
- Breakers and interrupters behave differently in a statistical sense regarding FE current intensity
- Statistically, longer arcing times at rated capacitive current show lower FE current than shorter arcing times. This is because of contact conditioning by the load current arc.
- Below approx. 10 kA inrush current peak, there is only a low FE current intensity.

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